Amendments to the Claims

1. (Original) A method of testing an electronic device including first and second semiconductor devices connected to each other with a plurality of bus lines, comprising the steps of:

the first semiconductor device supplying a selected one of the bus lines with a first logical output signal;

the second semiconductor device acquiring a first bus line signal from the selected bus line;

the second semiconductor device inverting the first bus line signal to generate a second logical output signal;

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the second semiconductor device transmitting the second logical output signal to the first semiconductor device;

the first semiconductor device receiving a second bus line signal from the selected bus line; and

the first semiconductor device comparing the first logical output signal and the second bus line signal to judge a connection between the first semiconductor device and the second semiconductor device.

2. (Original) The method of claim 1, wherein the first semiconductor device supplies the selected bus line with the first logical output signal having a first logical value, and supplies the other bus lines with signals each having a second logical value.

3. (Original) The method of claim 1, wherein the first semiconductor device supplies a first bus line adjacent to a second bus line with the first logical output signal

having a first logical value, and supplies the second bus line with a signal having a second logical value.

4. (Original) The method of claim 1, wherein the first semiconductor device supplies a first group of the bus lines adjacent to a second group of bus lines with the first logical output signals each having a first logical value, and supplies the second group of the bus lines with signals each having a second logical value.

5. (Original) The method of claim 1, wherein the steps of supplying the first logical output signal, acquiring the first bus line signal, and generating the second logical output signal are executed using the selected bus line.

6. (Original) A method of testing an electronic device including first and second semiconductor devices connected to each other with a plurality of bus lines, comprising the steps of:

the first semiconductor device supplying a selected one of the bus lines with a first logical output signal;

the second semiconductor device acquiring a first bus line signal from the selected bus line;

after outputting the first logical output signal, the first semiconductor device generating a second logical output signal being an inverted signal of the first logical output signal and supplying the selected bus line with the second logical output signal;

the second semiconductor device outputting the acquired first bus line signal;

the first semiconductor device receiving a second bus line signal from the selected bus line; and

the first semiconductor device comparing the first logical output signal and the received second bus line signal to judge a connection between the first semiconductor device and the second semiconductor device.

7. (Original) The method of claim 6, wherein the first semiconductor device supplies the selected bus line with the first logical output signal having a first logical value, and supplies the other bus lines with signals each having a second logical value.

8. (Original) The method of claim 6, wherein the first semiconductor device supplies a first bus line adjacent to a second bus line with the first logical output signal having a first logical value, and supplies the second bus line with a signal having a second logical value.

9. (Original) The method of claim 6, wherein the first semiconductor device supplies a first group of the bus lines adjacent to a second group of the bus lines with the first logical output signals each having a first logical value, and supplies the second group of the bus lines with signals each having a second logical value.

10. (Original) The method of claim 6, wherein the steps of supplying the first logical output signal, acquiring the first bus line signal, generating the second logical output signal, and outputting the acquired first bus line signal are executed using the selected bus line.

11. (Previously Amended) An electronic device comprising first and second semiconductor devices connected to each other with a plurality of bus lines, wherein the first semiconductor device includes:

a first output circuit connected to one of the bus lines for supplying the bus line with a first logical output signal, and

a comparison circuit connected to the bus line; and

the second semiconductor device includes:

an input circuit connected to the bus line for acquiring a first bus line signal, and

a second output circuit connected to the input circuit for inverting the first bus line signal to generate a second logical output signal, and supplying a corresponding bus line with the second logical output signal, wherein the comparison circuit receives a second bus line signal and compares the first logical output signal and the second bus line signal to generate a judgment signal regarding a connection between the first semiconductor device and the second semiconductor device.

12. (Previously Amended) The electronic device of claim 11, wherein the semiconductor device includes a plurality of first output circuits and one of the bus lines is a selected bus line, and the first output circuit corresponding to the selected bus line supplies the selected bus line with the first logical output signal having a first logical value, and the other first output circuits corresponding to the other bus lines supplies the other bus lines with signals having a second logical value.

13. (Previously Amended) The electronic device of claim 11, wherein the first semiconductor device includes a plurality of first output circuits and at least one bus line is adjacent to another bus line, and a first output circuit corresponding to the at least one bus line supplies the first bus line with the first logical output signal having a first

logical value, and a first output circuit corresponding to the another bus line supplies the another bus line with a signal having a second logical value.

14. (Previously Amended) The electronic device of claim 11, wherein the first semiconductor device includes a first group of first output circuits corresponding to a first group of the bus lines adjacent to the second group of the bus lines and a second group of the first output circuits corresponding to the second group of the bus lines, and wherein the first group supplies the first group of the bus lines with the first logical output signals each having a first logical value, and the second group supplies the second group of the bus lines with signals each having a second logical value.

15. (Original) The electronic device of claim 11, wherein the first output circuit is used in a test mode and a normal operation mode of the first semiconductor device.

16. (Original) The electronic device of claim 11, wherein the input circuit and the second output circuit are used in a test mode and a normal operation mode of the second semiconductor device.

17. (Original) The electronic device of claim 11, wherein the input circuit includes:

a latch circuit that latches the first logical output signal, and

a reset circuit connected to the latch circuit, that resets the latch circuit in response to one of the first logical output signal and a command signal.

18. (Previously Amended) An electronic device comprising first and second semiconductor devices connected to each other with a plurality of bus lines, wherein the first semiconductor device includes:

a first output circuit connected to one of the bus lines for supplying the bus line with a first logical output signal,

an inversion output circuit connected to the bus lines for supplying the bus line with a second logical output signal being an inverted signal of the first logical output signal after the first output circuit supplies the first logical output signal, and

a comparison circuit connected to the bus line; and

the second semiconductor device includes:

an input circuit connected to the bus line for acquiring a first bus line signal, and

a second output circuit connected to the input circuit for supplying a corresponding bus line with the first bus line signal, wherein the comparison circuit receives a second bus line signal and compares the first logical output signal and the second bus line signal to generate a judgment signal regarding a connection between the first semiconductor device and the second semiconductor device.

19. (Previously Amended) The electronic device of claim 18, wherein the first semiconductor device includes a plurality of first output circuits and one of the bus lines is a selected bus line, and the first output circuit corresponding to the selected bus line supplies the selected bus line with the first logical output signal having a first logical value, and the other first output circuits corresponding to non-selected bus lines supply the non-selected bus lines with signals each having a second logical value.

20. (Previously Amended) The electronic device of claim 18, wherein the first semiconductor device includes a plurality of first output circuits and at least one bus line

is adjacent to another bus line, and the first output circuit corresponding to the at least one bus line supplies the at least one bus line with the first logical output signal having a first logical value, and the first output circuit corresponding to the another bus line supplies the another bus line with a signal having a second logical value.

21. (Previously Amended) The electronic device of claim 18, wherein the first semiconductor device includes a first group of the first output circuits corresponding to a first group of the bus lines adjacent to a second group of the bus lines and a second group of the first output circuits corresponding to the second group of the bus lines, and wherein the first group supplies the first group of the bus lines with the first logical output signals each having a first logical value, and the second group supplies the second group of the bus lines with signals each having a second logical value.

22. (Original) The electronic device of claim 18, wherein the first output circuit is used in a test mode and a normal operation mode of the first semiconductor device.

23. (Original) The electronic device of claim 18, wherein the input circuit and the second output circuit are used in a test mode and a normal operation mode of the second semiconductor device.

24. (Original) A first semiconductor device that judges a connection between the first semiconductor device and a second semiconductor device connected thereto with the bus lines, the first semiconductor device comprising:

an output circuit connected to each bus line that supplies each bus line with a first logical output signal, wherein the second semiconductor device receives a first bus

line signal and supplies a bus line with a second logical output signal being an inverted signal of the first bus line signal; and

a comparison circuit connected to each bus line, that receives a second bus line signal and compares the first logical output signal and the second bus line signal to generate a judgement signal regarding the connection between the first semiconductor device and the second semiconductor device.

25. (Original) A first semiconductor device that judges a connection between the first semiconductor device and a second semiconductor device connected thereto with bus lines, the first semiconductor device comprising:

an output circuit connected to each bus line that supplies each bus line with a first logical output signal, wherein the second semiconductor device receives a first bus line signal;

an inversion output circuit connected to each bus line that supplies each bus line with a second logical output signal being an inverted signal of the first logical output signal after the output circuit supplying the first logical output signal; and

a comparison circuit connected to each bus line, that receives a second bus line signal and compares the first logical output signal and the second bus line signal to generate a judgement signal regarding the connection between the first semiconductor device and the second semiconductor device.

26. (Previously Amended) The electronic device of claim 11, wherein:

the input circuit comprises a latch circuit that receives a logical signal supplied from the measuring semiconductor device via one of the bus lines, and

the second output circuit comprises a logical circuit connected to the latch circuit that inverts the latched logical signal to generate an inverted logical signal.

27. (Previously Amended) The electronic device of claim 26, further comprising a reset circuit connected to the latch circuit, that resets the latch circuit in response to either the first logical output signal or a command signal on the bus line.

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28. (Previously Amended) An electronic device of claim 18, wherein:

the input circuit comprises a latch circuit, and

the second output circuit comprises a logical circuit connected to the latch circuit.

29. (Previously Amended) The electronic device of claim 28, further comprising a reset circuit connected to the latch circuit, that resets the latch circuit in response to either the first logical output signal or a command signal on the bus line.

30. (Currently Amended) A semiconductor device comprising:

input terminals,

output terminals,

an internal circuit,

first bus lines that connect the input terminals and the internal circuit, respectively,

second bus lines that connect the output terminals and the internal circuit, respectively, and

test circuits connected between ~~said input terminals and said output terminals via test signal transmission paths, wherein at least a part of said first bus lines or said second bus lines is shared by said test signal transmission paths~~ either the first bus lines and the output terminals, or the second bus lines and the input terminals, and wherein the ~~test circuit is~~ test circuits are activated in a test mode and ~~is~~ are deactivated in a normal operation mode in order to share the first bus lines or the second bus lines in both of the test mode and the normal operation mode.

31. (Original) The semiconductor device of claim 30, wherein each of the test circuit includes:

an input logical circuit connected to the input terminals; and

a bus drive circuit connected between the input logic circuit and the second bus line.

32. (Original) The semiconductor device of claim 31, wherein the input logic circuit is physically located close to the input terminals, and the bus drive circuit is physically located close to the second bus line.

33. (Original) The semiconductor device of claim 31, wherein the bus drive circuit includes:

two PMOS transistors connected in series between a high potential power supply and the second bus line; and

two NMOS transistors connected in series between a low potential power supply and the second bus line, and wherein an activation signal of the bus drive circuit is

supplied to the gate of the PMOS transistor closing to the high potential power supply and the gate of the NMOS transistor closing to the low potential power supply.

34. (Original) The semiconductor device of claim 30, further comprising clamp circuits connected to the respective input terminals, that clamp the input terminals to a specific potential.

35. (Original) The semiconductor device of claim 34, wherein the clamp circuits clamp the input terminals to the specific potential in a test mode, and release the clamp in a normal operation mode.

36. (Original) The semiconductor device of claim 34, wherein the clamp circuits are controlled by an activation signal of the test circuit.

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37. (Original) The semiconductor device of claim 34, wherein the clamp circuits include a MOS transistor, and the gate of the MOS transistor is supplied with an inverted signal of the potential level at the corresponding input terminal.

38. (Original) The semiconductor device of claim 34, wherein the clamp circuits are controlled by a power-on signal and an activation signal of the test signal.

39. (Original) The semiconductor device of claim 34, wherein the clamp circuits are controlled by a power-on signal and a normal mode signal.

40. (Original) The semiconductor device of claim 39, wherein the normal mode signal is generated on the basis of detecting an operation conducted when power is turned on.

41. (Original) The semiconductor device of claim 40, wherein the operation conducted when the power is turned on includes at least one of a pre-charge operation, a mode setting operation, and a refresh operation.

42. (Original.) The semiconductor device of Claim 34, wherein each input terminal includes a terminal that receives a chip select signal.

43. (Original.) The semiconductor device of claim 34, wherein each input terminal includes a terminal that receive a column address strobe signal.

44. (Original) The semiconductor device of claim 34, wherein each input terminal includes a terminal that receives a clock enable signal.

45. (Original) The semiconductor device of claim 34, wherein the clamp circuits clamp at least one input terminal to an inverted potential level of the specific potential level supplied to the one input terminal when entering the test mode.

46. (Original) The semiconductor device of claim 34, wherein the clamp circuit includes a latch circuit that holds the specific potential level when the power is turned on, and the clamp circuit clamps the input terminal to the specific potential level held by the latch circuit.

47. (Currently Amended) A semiconductor device comprising:

input terminals,

output terminals,

an internal circuit,

test circuits connected between the input terminals and the output terminals, and

clamp circuits connected to the input terminals, that clamp the respective input terminals to a specific potential that is different from a potential of a test mode signal provided to the respective input terminals in a test mode, and release the clamp of the input terminals in a normal operation mode.

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48. (Original) The semiconductor device of claim 30, further comprising output buffer circuits to receive output signals from said internal circuit in a first operation mode, receive test signals from said test circuits in a second operation mode, and output buffer output signals to said output terminals.